REMARKS

Applicants respectfully request reconsideration of the Office Action mailed December 23, 2003. Claims 1-52 remain presented for examination. Claims 35-52 have been withdrawn from consideration.

In addition, Applicants respectfully note that the Information Disclosure Statement which was filed with this application has not been acknowledged and has not yet been made of record.

Restriction Requirement

Restriction to one of the following two groups of claims is required under 35 U.S.C. § 121: (I) Claims 1-34, drawn to a method of making a semiconductor device; and (II) Claims 35-52, drawn to a semiconductor device.

Applicants hereby affirm the election made by Applicants during a telephone conversation on December 9, 2003. Specifically, Applicants affirm the election of Group I, Claims 1-34.

Rejection of Claims 1 and 8-9 under 35 U.S.C. § 102(b) over Ishikawa

Claims 1 and 8-9 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,239,016 to Ishikawa. Applicants respectfully traverse this rejection.

The invention defined by Claim 1 is directed to a method of forming an interconnect structure on a substrate. The method comprises the steps of: depositing at least one dielectric layer on the substrate, the dielectric layer being formed of at least one first dielectric material; embedding at least one conductive interconnect in the dielectric layer, the conductive interconnect having sidewalls in contact with the first dielectric material; removing a portion of the first dielectric material in selected areas of the dielectric layer, thereby forming at least one opening in the dielectric layer, such that the sidewalls of the conductive interconnect remain in contact with the first dielectric material; and filling the opening with a second dielectric material. It is therefore a

feature of this invention that the dielectric layer is deposited first, and then the conductive interconnect is embedded in the dielectric layer, in a typical damascene process. Applicants respectfully submit that this feature is not disclosed by Ishikawa, as follows.

The Ishikawa patent is directed to multilevel interconnects in a semiconductor device and a method for forming the same. The method begins with formation of the interconnections, and then the dielectric material is formed to cover the interconnections (col. 5, lines 35-43), in a typical subtractive patterning process. Ishikawa fails to disclose formation of an interconnect structure using a damascene process, wherein the dielectric layer is deposited first and then the conductor is embedded in the dielectric layer.

Since Ishikawa fails to disclose the above-identified feature of Claim 1, Applicants respectfully submit that Claim 1 is not anticipated by the Ishikawa patent. Claims 8-9, which include all of the limitations of Claim 1, also are not anticipated by the Ishikawa patent. Applicants therefore request withdrawal of this rejection.

Rejection of Claims 1-8, 21 and 26 under 35 U.S.C. § 102(b) over Grill et al.

Claims 1-8, 21 and 26 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,413,852 to Grill et al. Applicants respectfully traverse this rejection.

As discussed previously, the invention defined by Claim 1 is directed to a method of forming an interconnect structure on a substrate. The method comprises the steps of: depositing at least one dielectric layer on the substrate, the dielectric layer being formed of at least one first dielectric material; embedding at least one conductive interconnect in the dielectric layer, the conductive interconnect having sidewalls in contact with the first dielectric material; removing a portion of the first dielectric material in selected areas of the dielectric layer, thereby forming at least one opening in the dielectric layer, such that the sidewalls of the conductive interconnect remain in contact with the first dielectric material; and filling the opening with a second dielectric material. It is therefore a feature of this invention that after a portion of the first dielectric material

has been removed to form an opening in the dielectric layer, the opening is filled with a second dielectric material. Applicants respectfully submit that this feature is not disclosed by Grill et al., as follows.

The Grill et al. patent is directed to a method of forming a multilevel interconnect structure containing air gaps. The method begins with formation of a dielectric layer 110-140 (Figs. 1A-1B), and then conductor 185 is embedded in the dielectric layer (Figs. 1C-1E). A portion of the dielectric layer is then removed, to form openings 190 (Fig. 1F). These openings, however, are not filled with a second dielectric material. Rather, the structure is filled with a sacrificial place-holder (SPH) material 220 (Fig. 1H), which is then extracted to form the structure having air gaps (Fig. 1N). Grill et al. fail to disclose a method wherein the opening in the dielectric layer is filled with a second dielectric material.

Since Grill et al. fail to disclose the above-identified feature of Claim 1, Applicants respectfully submit that Claim 1 is not anticipated by the Grill et al. patent. Claims 2-8, 21 and 26, which include all of the limitations of Claim 1, also are not anticipated by the Grill et al. patent. Applicants therefore request withdrawal of this rejection.

Claim 1 is not anticipated by the Grill et al. patent for the following additional reason. It is another feature of this invention that after a portion of the first dielectric material has been removed to form an opening in the dielectric layer, sidewalls of the conductive interconnect remain in contact with the first dielectric material. Applicants respectfully submit that this feature is not disclosed by Grill et al., as follows.

The Grill et al. method is similar to the prior art method shown in Figures 5(a)-5(e) and discussed in paragraphs 4-5 of the present application. The Grill et al. method begins with a typical dual damascene structure (Fig. 1E), which is then etched back so as to expose regions of in-laid wiring 185 (Fig. 1F). Thus, after a portion of the dielectric layer has been etched back, sidewalls of the conductive wiring do ***not*** remain in contact with the dielectric material.

Since Grill et al. fail to disclose the above-identified additional feature of Claim 1, Applicants respectfully submit that Claim 1 is not anticipated by the Grill et al. patent. Claims 2-8, 21 and 26, which include all of the limitations of Claim 1, also are not anticipated by the Grill et al. patent. For this additional reason, Applicants request withdrawal of this rejection.

Rejection of Claims 10-20, 22-25 and 27-34 under 35 U.S.C. § 103(a) over Grill et al.

Claims 10-20, 22-25 and 27-34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Grill et al. Applicants respectfully traverse this rejection.

Claims 10-20, 22-25 and 27-34 all depend ultimately from Claim 1. As discussed previously, it is a feature of the invention defined by Claim 1 that after a portion of the first dielectric material has been removed to form an opening in the dielectric layer, sidewalls of the conductive interconnect remain in contact with the first dielectric material. Applicants respectfully submit that this feature not only is not disclosed but also is not suggested by Grill et al., as follows.

The Grill et al. method is similar to the prior art method shown in Figures 5(a)-5(e) and discussed in paragraphs 4-5 of the present application. The Grill et al. method begins with a typical dual damascene structure (Fig. 1E), which is then etched back so as to expose regions of in-laid wiring 185 (Fig. 1F).

This method suffers from the following drawbacks. First, the conductive wiring is exposed during the etchback, which could result in erosion. Second, the copper conductor may undergo silicidization during exposure to the etchback process, resulting in higher resistivity. Finally, exposing the sidewalls of the conductive wiring during etchback of the first dielectric material may result in loss of wire sidewall mechanical support, which may cause the wire to "flop over" or may cause other mechanical integrity issues.

Grill et al. recognize the problem of potential damage to the conductive wiring during etchback, but they propose addressing that problem by adding an additional repair step involving selectively depositing an electroless metal barrier material on exposed wiring surfaces (col. 6, lines 10-14). Grill et al. fail to recognize

that this problem may be eliminated by performing the etchback such that sidewalls of the conductive interconnect remain in contact with the first dielectric material. Grill et al. therefore provide no motivation to modify their method to include the above-identified feature.

Accordingly, Applicants respectfully submit that Claims 10-20, 22-25 and 27-34, which include all of the limitations of Claim 1, are patentable over the Grill et al. patent. Applicants therefore request withdrawal of this rejection.

Claims 10-20 are patentable over the Grill et al. patent for the following additional reason. These claims are directed to two embodiments of the present invention, which are illustrated in Figures 1(a)-1(d) and 2(a)-2(d). In these embodiments, the portion of the first dielectric material is removed by a method comprising the steps of: forming a cap on each conductive interconnect, the cap having a lateral extent greater than that of the conductive interconnect, thereby masking portions of the dielectric layer adjacent to the conductive interconnect and leaving other portions of the dielectric layer not masked; and removing a portion of the first dielectric material in areas of the dielectric layer not masked by the cap, thereby forming the opening in the dielectric layer. It is therefore a feature of these embodiments that the cap formed on each conductive interconnect masks portions of the dielectric layer adjacent to the conductive interconnect, such that the sidewalls of the conductive interconnect remain in contact with the first dielectric material. Applicants respectfully submit that this feature is neither disclosed nor suggested by Grill et al.

As discussed previously, Grill et al. fail to disclose or even suggest performing the etchback such that sidewalls of the conductive interconnect remain in contact with the first dielectric material. In fact, Grill et al. teach that the etchback is preferably performed with an anisotropic etch process, using the conductive wiring structures as a mask (col. 5, lines 58-60). Grill et al. therefore provide no motivation to modify their method to use a cap having a lateral extent greater than that of the conductive interconnect as a mask.

For this additional reason, Applicants respectfully that Claims 10-20 are patentable over the Grill et al. patent, and therefore request withdrawal of this rejection.

Claims 22-25 and 27-34 are patentable over the Grill et al. patent for the following additional reason. These claims are directed to another two embodiments of the present invention, which are illustrated in Figures 3(a)-3(f) and 4(a)-4(f). In these embodiments, the conductive interconnect has a top portion with a lateral extent greater than that of lower portions of the interconnect, thereby masking areas of the first dielectric material, and the first dielectric material is removed in areas not masked by the top portion of the conductive interconnect. It is therefore a feature of these embodiments that the conductive interconnect has a top portion with a lateral extent greater than that of lower portion of the interconnect, thereby masking portions of the dielectric layer adjacent to the conductive interconnect, such that the sidewalls of the conductive interconnect remain in contact with the first dielectric material. Applicants respectfully submit that this feature is neither disclosed nor suggested by Grill et al.

As discussed previously, Grill et al. fail to disclose or even suggest performing the etchback such that sidewalls of the conductive interconnect remain in contact with the first dielectric material. Even where etchback is performed using the conductive wiring as a mask, Grill et al. teach that the etchback may be performed using an isotropic etch process, to undercut the dielectric line supports (col. 5, lines 60-64). Grill et al. therefore provide no motivation to modify their method to use a conductive interconnect having a top portion with a lateral extent greater than that of lower portions as a mask.

For this additional reason, Applicants respectfully that Claims 22-25 and 27-34 are patentable over the Grill et al. patent, and therefore request withdrawal of this rejection.

Conclusion

Applicants have properly traversed each of the grounds for rejection in the Office Action, and therefore submit that the present application is now in condition for allowance. If the Examiner has any questions or believes further discussion will aid examination and advance prosecution of the application, a telephone call to the undersigned is invited.

No fee is believed to be due for the submission of this amendment. If any fees are required, however, the Commissioner is authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,

Margaret A. Pepper

Margaret A. Pepper
Attorney for Applicant
Reg. No. 45,008

Phone: (845) 894-4713
Fax: (845) 892-6363
e-mail: mpepper@us.ibm.com